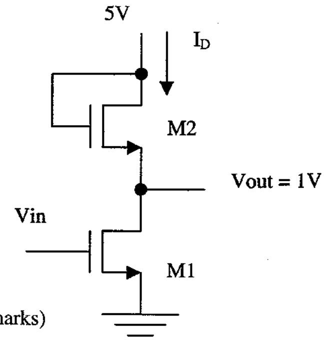
2. The MOS transistors M1 and M2 are identical.
Given : $K = 10\ mA/V^2$ and $V_T = 1V$.

$$I_D = K(V_{GS} - V_T)^2 \qquad \textit{Saturation}$$

$$I_D = 2K\left[(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^{\ 2}}{2}\right] \qquad \textit{Ohmic}$$



a) Find and prove the operation mode of M2. (6 marks)
b) Calculate the current I_D. (4 marks)
c) Find Vin if M1 is in ohmic. (7 marks)
d) Estimate the ON resistance ron of M1 (ron = $\partial V_{DS} / \partial I_D$). (5 marks)

a) $V_{GS} > V_T$ $\qquad V_{DS} > V_{GS} - V_T$

$5 - 1 > 1$ $\qquad 4 > 4 - 1$

$\therefore$ M2 is saturate $\qquad$ 6

b) $I_D = K(V_{GS} - V_T)^2 = 10m(4-1)^2 = 90mA$ $\qquad$ 4

c) $I_D = 2K\left[(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}\right]$

$90m = 2(10m)\left[(V_{in} - 1)1 - \frac{1}{2}\right]$

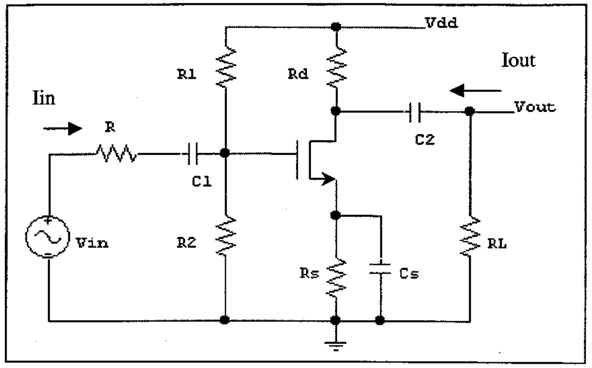
$4.5 = V_{in} - 1.5$

$\therefore V_{in} = 6V$ $\qquad$ 7

d) $r_{on} \doteq \frac{1}{2K(V_{GS} - V_T)} = \frac{1}{2(10m)(6-1)}$ $\qquad$ 5

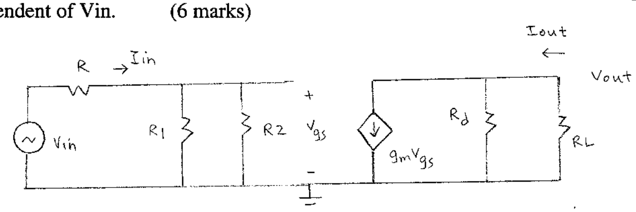
$= 10\Omega$

3. Given the following circuit diagram.



a) Draw the ac equivalent circuit for the whole circuit. Assume C1, C2 and Cs are large, and r_o of NMOS model is infinity. (7 marks)
b) Find the total input resistance Rin (Rin = Vin / Iin). (3 marks)
c) Find the total output resistance Rout (Rout = Vout / Iout). (3 marks)
d) Find the ac voltage gain of the amplifier (Av = Vout / Vin). The expression is required to be independent of Vin. (6 marks)

a)



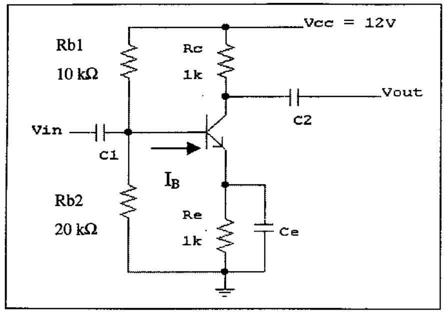
7

b) $R_{in} = \frac{V_{in}}{I_{in}} = R + R_1 \,//\, R_2$ $\qquad$ 3

c) $R_{out} = R_L$ $\qquad$ 3

d) $A_V = \frac{V_{out}}{V_{in}} = \frac{-g_m V_{gs}\,(R_d \,//\, R_L)}{\frac{V_{gs}}{R1 // R2}(R + R1 // R2)}$ $\qquad$ 6

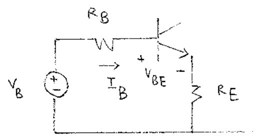
12. Given the following circuit diagram.



$\beta = 50$
V_{CE} (sat) = 0.2 V
$V_{BE} = 0.7$ V

a) Show that the base current I_B is 0.127 mA. (Hint : Use Thevenin's Theorem) (13 marks)
b) Show that the Q-point is in the saturation region. (8 marks)
c) Show that the forced β is 29.7 (18 marks)
d) Suggest a method to move the Q-point to the active region. (4 marks)
e) Give two advantages of this circuit connection. (4 marks)
f) Briefly explain the function of C1, C2 & Ce. (5 marks)

a)



$V_B = V_{cc} \dfrac{R_{b2}}{R_{b1} + R_{b2}} = 12 \dfrac{20K}{10K + 20K} = 8V$ 3

$R_B = R_{b1} \parallel R_{b2} = 10K \parallel 20K = \dfrac{20K\Omega}{3}$ 3

$I_B = \dfrac{V_B - V_{BE}}{R_B + (1+\beta) R_E} = \dfrac{8 - 0.7}{\frac{20K}{3} + (1+50)1k}$

$= 0.127$ mA 7

b) If BJT active, $I_c = \beta I_B = 50 \, (0.127 m)$

$= 6.33$ mA $\approx I_E$

but $I_c R_c + I_E R_E \approx 6.33 m \, (2k)$

> 12 V

∴ BJT saturates 8

c) BJT saturates

$V_{cc} = I_c R_c + V_{CESAT} + I_E R_E$

$12 = \beta_f I_B \, 1K + 0.2 + (1 + \beta_f) I_B \, 1K$

$\therefore I_B = \dfrac{11.8}{1K \, (2\beta_f + 1)}$

But I_B also $= \dfrac{V_B - V_{BE}}{R_B + (1+\beta_f) R_E} = \dfrac{8 - 0.7}{\frac{20k}{3} + (1+\beta_f)1k}$

$\therefore 7.3K\,(1 + 2\beta_f) = 11.8K\,(\frac{20}{3} + 1 + \beta_f)$

$\therefore \beta_f = 29.7$ 18

d) BJT active, $I_B \downarrow$

or $R_B + (1+\beta) R_E \uparrow$ 4

e) single supply (V_{cc})

stable Q point 4

f) C_1 C_2 : block DC and

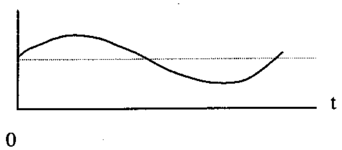
pass AC current 5

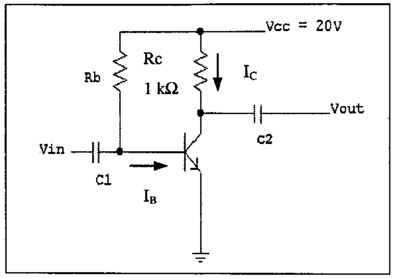
C_e : short R_E at AC

increase A_V

13. Given the following circuit diagram. The input (base) and output (collector) characteristics of the BJT are given.

Vin = 0.71 + 0.05 sin ωt V





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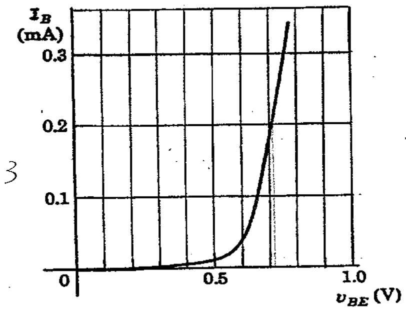
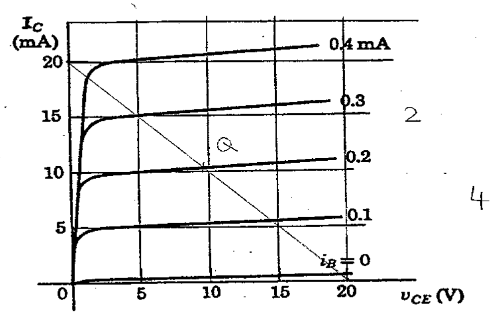


(a) Base characteristics



(b) Collector characteristics

a) Plot the dc load line in the output characteristics. Show clearly your calculations. (4 marks)
b) Show that the base current I_B is 0.2 mA. (3 marks)
c) Calculate Rb. (3 marks)
d) Show the location of the Q-point in the output characteristics. (2 marks)
e) Find Ic and V_{CE} at the Q-point. (4 marks)
f) Sketch the base current I_B, the collector current I_C and the output voltage Vout. Show clearly the dc level, the maximum and the minimum values in your sketch. (15 marks)
g) Calculate the ac voltage gain (Av = Δ Vout / ΔVin). (3 marks)
h) Calculate the ac current gain (Ai = ΔIc / ΔI_B). (3 marks)

a) $V_{cc} = I_c R_c + V_{CE}$

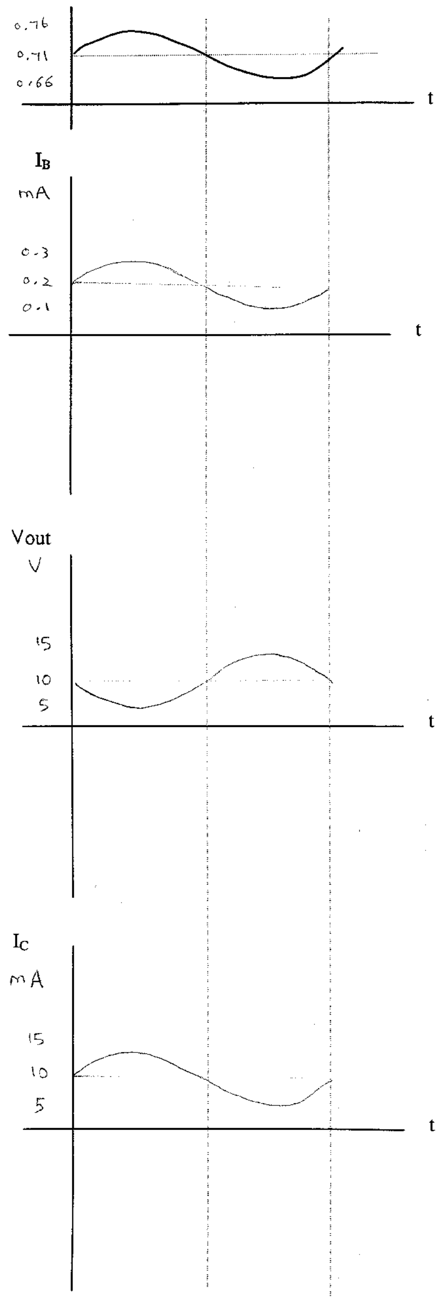
$I_c = 0 \qquad V_{CE} = V_{cc} = 20\text{ V}$

$V_{CE} = 0 \qquad I_c = \frac{V_{cc}}{R_c} = \frac{20\text{ V}}{1k} = 20\text{ mA}$

b) $V_{BE} \approx 0.7\text{ V}$

$I_B = 0.2\text{ mA}$ 3

Vin = 0.71 + 0.05 sin ωt V



c) $R_b = \frac{V_{cc} - V_{BE}}{I_B}$

$= \frac{20 - 0.7}{0.2m}$

$= 96.5\text{ k}\Omega$ 3

d) Q point

e) $I_c \approx 10\text{ mA}$ 4

$V_{CE} \approx 10\text{ V}$

f) 15

g) $A_V = \frac{\Delta V_{out}}{\Delta V_{in}}$

$\approx \frac{5 - 15}{0.76 - 0.66}$ 3

$= -100$

$A_I = \frac{\Delta I_c}{\Delta I_B}$

$\approx \frac{15 - 5}{0.3 - 0.1}$ 3

$= 50$

END

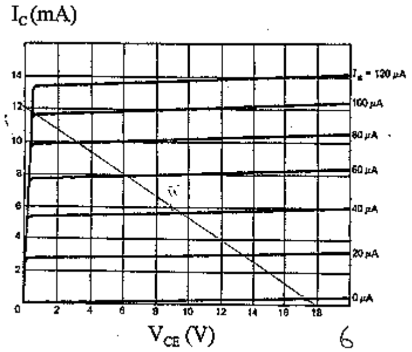
12. The BJT in the circuit has the output characteristic curves as shown.

(a) Sketch the load line $V_{CC} = I_C R_C + V_{CE}$. (6)

(b) Locate the Q-point on the loadline and find the operating modes of the BJT (i) if Vi = 0.8V, and (ii) if the circuit is to give maximum symmetric V_{CE} output. (14)

(c) Show that the voltage gain A_V (= ΔVo /ΔVi) of the circuit is -90. (11)

Given that for the BJT, $V_{BE} = 0.7V$, $\beta = 120$, $r_\pi = 1\ k\Omega$, $r_o = \infty$.



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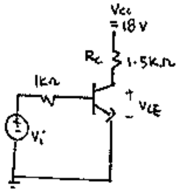


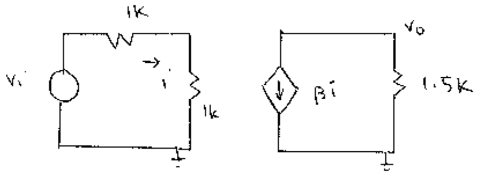
(i) $V_i = 0.8V$

$$I_B = \frac{0.8 - 0.7}{1k} = 0.1m$$ 4

BJT ON. 3

(ii) middle of load line 4

BJT active 3



$$\therefore A_V = \frac{V_o}{V_i} = -\frac{\beta i(1.5k)}{i(2k)}$$

$$= -120\frac{(1.5)}{2} = -90$$ 11

13. (a) Show that $\overline{AB} + A\overline{B} = \overline{AB}$ using Boolean algebra. (7)

$$\overline{AB} + A\overline{B}$$

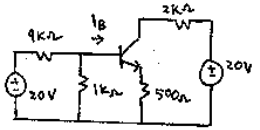
$$= \bar{A} + \bar{B} + A\bar{B}$$

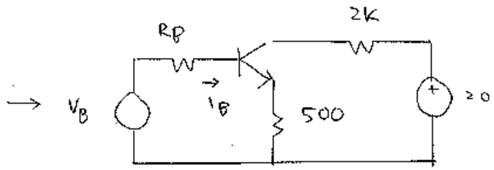
$$= \bar{A} + \bar{B}(1 + A)$$

$$= \bar{A} + \bar{B}$$

$$= \overline{AB}$$ 7

11. In the circuit, (a) show that $I_B \sim 25\ \mu A$. (19)
(b) Explain briefly why the circuit can have stable Ic. (7)
For the BJT, given $V_{BE} = 0.7V$ and $\beta = 100$.





$V_B = 20 \frac{1K}{10K} = 2V$ 5

$R_B \doteq 1K \| 9k = 900\ \Omega$ 4

$\therefore\ 2 = I_B R_B + V_{BE} + I_E 500$

$= I_B 900 + 0.7 + (101) I_B 500$

$\therefore\ I_B = \frac{2 - 0.7}{900 + 101(500)} \doteq 25\ \mu A$ 10

$I_C \uparrow \quad V_E \uparrow \quad V_{BE} \downarrow \quad I_B \downarrow \quad I_C \downarrow$ 7

16. Two T-FFs are used to construct a synchronous counter as shown below. T_B, T_A and Q_B, Q_A are the inputs and outputs of the T-FFs. Complete the state table for the counter, find the logic functions for T_A and T_B, and hence draw the circuit of the counter. (20)

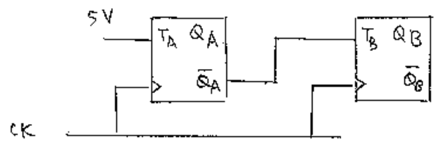
Present State		Next State		T inputs	
Q_B	Q_A	Q_B	Q_A	T_B	T_A
0	0	1	1	1	1
0	1	0	0	0	1
1	1	1	0	0	1
1	0	0	1	1	1

8

$T_B = \bar{A}$

$T_A = 1$

6



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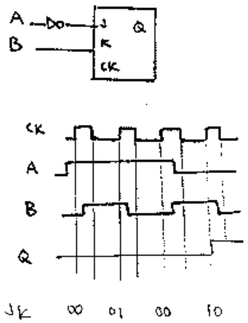
End of Paper! Merry Christmas, Happy 2000, and very successful future!

(b) Express decimal number 8.25 in binary form. (6)

$8.25_{10} = 1000.01_2$

6

14. Write the truth table for the following JKFF and sketch the waveform of Q. Q is 0 initially. (12)



J	K	Q
0	0	Q_0
0	1	0
1	0	1
1	1	$\overline{Q}_0$

4

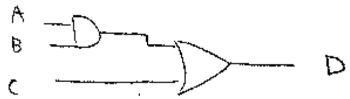
8

15. A logic circuit has 3 inputs ABC and 1 output D. D is 0 when ABC are 000, 010 and 100 and is 1 for other inputs. Design the logic circuit using <u>2-input NAND gates only</u>. (18)

C \ AB	00	01	11	10
0			1	
1	1	1	1	1

$\therefore D = AB + C$

10



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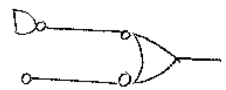

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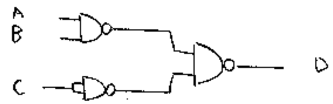

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